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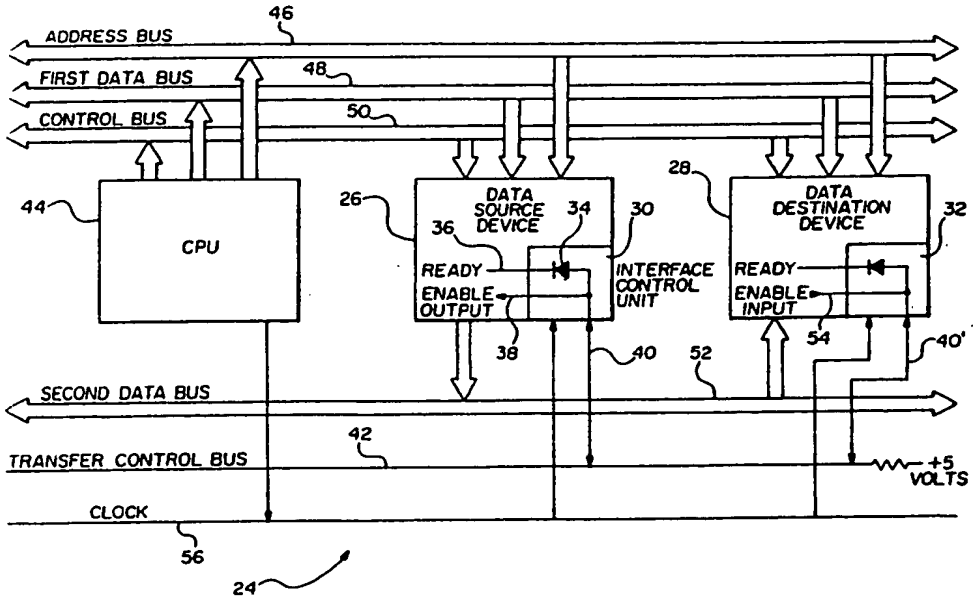

(57) Abstract

A novel electrical bus structure suitable for use in an integrated, portable image processing system. The bus structure provides an interface between components of the image processing system, the components comprising a data source device and data destination device. The bus structure has concurrent capabilities of realizing very high speeds of data transmission and very low power consumption.

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NOVEL ELECTRICAL BUS STRUCTURE

BACKGROUND OF THE INVENTION

This invention relates to an electrical bus structure.

INTRODUCTION TO THE INVENTION

An electrical bus structure is a known and important entity that can function, for example, in a modular image processing system, as an interface between, on the one hand, a data source device including e.g., memory devices, encryption devices or transmission devices, and on the other hand, a data destination device, including e.g., memory devices, compression devices or displays.

Fig. 1 shows a typical electrical bus structure 10. The bus structure 10 can function as an interface between a data source device 12 and a data destination device 14. To this end, the bus structure 10 further includes a controller 16 i.e., a conventional central processing unit (CPU), and address bus lines 18, data bus lines 20, and control bus lines 22. The bus structure further includes sundry interconnect lines between the three sets of bus lines 18, 20, 22, and the controller 16 and source and destination devices 12, 14, respectively.

In operation, the Fig. 1 bus structure 10 can transfer a datum from the data source device 12, to the data destination device 14, by way of a two-step process. First, the controller 16 can generate an address, by way of well-known read command instructions along the control bus line 22, to the data source 12, thereby specifying the address of the datum to be transferred by the bus 10. Second, the controller 16 can generate an

address, by a way of well-known write command instructions along the control bus line 22, to the data destination device 14, thereby specifying the address in the data destination device 14 to which the datum is to be now transferred along the data bus lines 20.

SUMMARY OF THE INVENTION

The operation of the Fig. 1 bus structure 10 conforms, generally, to a speed transmission vs. power consumption curve shown in Fig. 2. The Fig. 2 curve suggests that the speed of data transmission is directly proportional to the power requirements of the bus structure.

Accordingly, for the Fig. 1 bus structure 10, increased speed of data transmission may be accommodated, for example, by way of adding extra data bus lines to the structure 10, (as shown), to thereby (incrementally) handle 8, 16, 32, 64 ... bit capacities. However, this action is at the expense or trade-off of increased power consumption. On the other hand, Fig. 2 suggests that a relative reduction in the Fig. 1 bus structure power consumption requires a corresponding diminution in the speed of the data transmission. (This trade-off of speed versus power, is in part a consequence of the two-step controller addressing process, alluded to above.)

Heretofore, a bus structure that operates in accordance with the Fig. 2 speed/power curve, has been acceptable for use in modular image processing systems, since the data source and data destination devices typically comprise large, heavy and independent units. These non-portable units can be adequately equipped with A.C. power supplies typically rated in excess of 200 watts power

consumption, to thereby accommodate a satisfactory speed of data transmission.

In contrast to the modular image processing systems, and their acceptable speed/power specifications, I am now required to design a bus structure that is suitable for use as an interface between data source and destination devices for a small, portable and integrated image processing system. The integrated system is specified to be not only small (e.g., less than 10 pounds), but have a power consumption of less than 5 watts, while retaining the data speed capabilities of at least that of the modular image processing systems.

For this situation, I have determined that the extant bus structure architectures, while suitable for the modular image processing systems, may not be viable for the portable integrated system. This follows since the extant bus structures conform to the Fig. 2 speed/power trade-offs, while the portable integrated system, in sharp contrast, must realize high speed concurrently with very low power consumption.

I have now invented a novel electrical bus structure that can provide an interface between data source and data destination devices, and that is suitable for use in an integrated, portable image processing system. The novel electrical bus structure has a critical advantage of facilitating the advent of portable image processing systems that can preserve all the features and capabilities of large-scale modular image processing systems, including high speeds of data transmission, for example, image data transmission, while at the same time, dispensing with the heretofore seemingly dictated (Fig. 2) high power consumption supply, in

favor of a portable, low power (A.C. or D.C.) supply, e.g., less than 5 watts, battery-operated supply.

The novel electrical bus structure comprises:

a) a controller comprising a central processing unit (CPU);

b) a data source device comprising an interface control unit;

c) a data destination device comprising an interface control unit;

d) an address bus that can connect

i) the CPU and the data source device; and

ii) the CPU and the data destination device;

e) a first data bus that can connect

i) the CPU and the data source device; and

ii) the CPU and the data destination device;

f) a control bus that can connect

i) the CPU and the data source device; and

ii) the CPU and the data destination device;

g) a second data bus that can connect the data source device to the data destination device; and

h) a transfer control bus that can connect the control unit of the data source device to the control unit of the data destination device.

BRIEF DESCRIPTION OF THE DRAWING

The invention is illustrated in the accompanying drawing, in which:

Fig. 1 shows an extant electrical bus structure;

Fig. 2 shows an electrical bus structure function comprising a speed of data transmission versus power consumption curve;

Fig. 3 shows a novel electrical bus structure of the present invention; and

Fig. 4 shows a flowchart incorporated in an operation of the Fig. 3 bus structure.

DETAILED DESCRIPTION OF THE INVENTION

A detailed description of a preferred electrical bus structure of the present invention, as summarized above, is first set forth with reference to Fig. 3. The operation of the Fig. 3 bus structure is then disclosed, with particular attention to the Fig. 4 flowchart.

The Fig. 3 shows a preferred bus structure 24. The bus structure can function as an interface between at least one data source device 26 comprising, for example, a memory device or an encryption device, and at least one data destination device 28 comprising, for example, a compression device, a display or a memory device.

The data source device 26 and the data destination device 28 each include an interface control unit (numerals 30, 32). The illustrative interface control unit 30 preferably comprises at least one conventional diode circuit 34, comprising a "Ready" signal input line 36 (i.e., a signal which is "True" when the data source device 26 is ready to output a datum), an "Enable" signal output line 38 (i.e., a signal which enables the data source device 26 to output a datum), and an interconnect line 40 (40') to a transfer control bus 42. Note that the

interface control units 30, 32 act cooperatively with the transfer control bus 42, to function as a wired AND gate.

Fig. 3 shows that the electrical bus structure 24 further includes a controller 44 comprising a conventional central processing unit (CPU). The controller 44 can communicate with the data source device 26 and the data destination device 28 by way of an address bus 46, a first data bus 48, and a control bus 50.

The Fig. 3 bus structure 24 is completed by noting firstly that the interface control units 30, 32 of the data source device 26 and the data destination device 28, respectively, can directly communicate by way of a second data bus 52. In particular, the "Enable" signal output line 38 is connected via the second data bus 52 to an "Enable" signal input line 54 in the interface control unit 32. Secondly, an optional clock line 56 can be provided for synchronous coordination of a data flow.

The operation of the Fig. 3 bus structure 24, in overview, is as follows.

First, the controller 44 may be programmed so that it can dedicate low speed data transmission (hence low power consumption) to that part of the bus structure 24 comprising the address bus 46, the first data bus 48, and the control bus 50. Further, a low speed datum may be processed by the controller 44 along these routes (46, 48, 50) from the data source device 26 to the data destination device 28, and by the two stage process described above for the bus structure 10 shown in Fig. 1. As noted above, the two-stage process is relatively slow, but since a low speed datum has been assigned to this process, there is no overall loss of efficiency; at the same

time, the power consumption is kept desirably low.

Second, the controller 44 may be programmed so that it can dedicate the transfer of high speed data, for example, image data, again initially by way of the address bus 46, the first data bus 48, and the control bus 50, but now with a further constraint that a high speed datum is only to be transferred from the data source device 26 to the data destination device 28 by way of the interface control units 30, 32 and the second data bus 52. The transfer takes place via the wired AND gate logic disclosed above, and therefore the transfer of the datum takes place when all the "Ready" signal input lines are (preferably) logic high. Since the transfer takes place, accordingly, as a one step wired AND gate process, the transfer of high speed data can be effected concurrently with a desirable low power consumption.

Attention is now directed to the Fig. 4 flowchart 58, which references this operation. The flowchart 58 comprises a program that can be effected by the Fig. 3 controller 44.

An instruction 60 comprises that the controller 44 load a data source device 26 address. An instruction 62 comprises that the controller 44 enables the data source device 26.

A further instruction 64 comprises that the controller 44 loads a data destination device 28 address. An instruction 66 comprises that the controller 44 enables the data destination device 28.

The final flowchart instruction 68 signifies that when all the enablements are effected, a transfer of at least one datum occurs along the second data bus 52, and with synchronization with the logic on the transfer

control bus 42.

WHAT IS CLAIMED IS:

1. An electrical bus structure comprising:

a) a controller comprising a central processing unit (CPU);

b) a data source device comprising an interface control unit;

c) a data destination device comprising an interface control unit;

d) an address bus that can connect

i) the CPU and the data source device; and

ii) the CPU and the data destination device;

e) a first data bus that can connect

i) the CPU and the data source device; and

ii) the CPU and the data destination device;

f) a control bus that can connect

i) the CPU and the data source device; and

ii) the CPU and the data destination device;

g) a second data bus that can connect the data source device to the data destination device; and

h) a transfer control bus that can connect the control unit of the data source device to the control unit of the data destination device.

2. An electrical bus structure according to claim 1, wherein the data source device comprises a memory.

3. An electrical bus structure according to claim 1, wherein the data destination device comprises a display.

4. An electrical bus structure according to claim 1, wherein a wired AND gate circuit comprises

a) the transfer control bus;

b) the control unit of the data source device;

and

c) the control unit of the data destination device.

5. An electrical bus structure according to claim 4, wherein the wired AND gate circuit comprises a diode circuit.

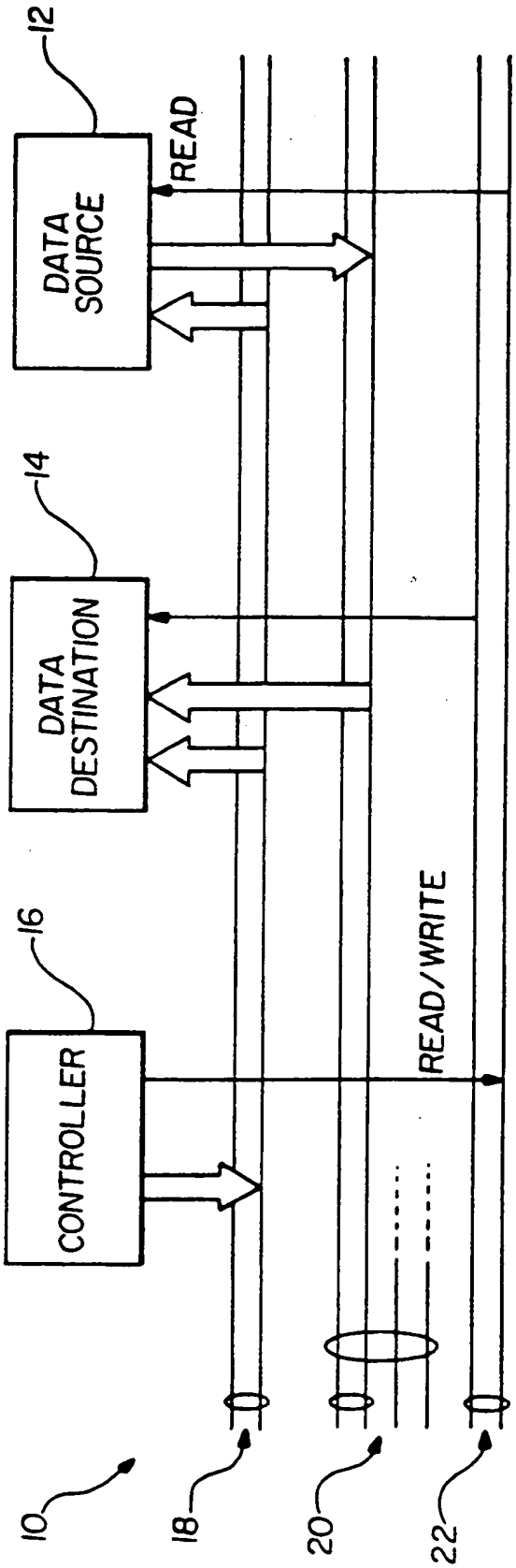
12
DATA SOURCE
READ
14
DATA DESTINATION
16
CONTROLLER
READ/WRITE
10
18
20
22

FIG. 1

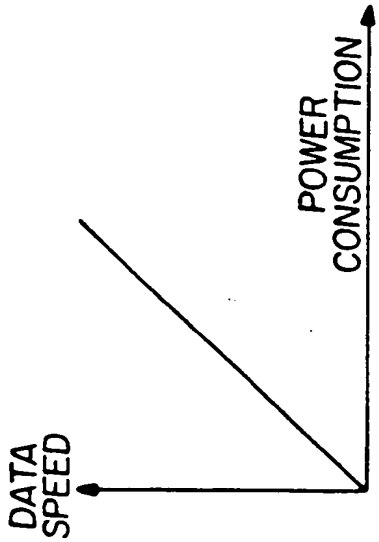
POWER CONSUMPTION
DATA SPEED

FIG. 2

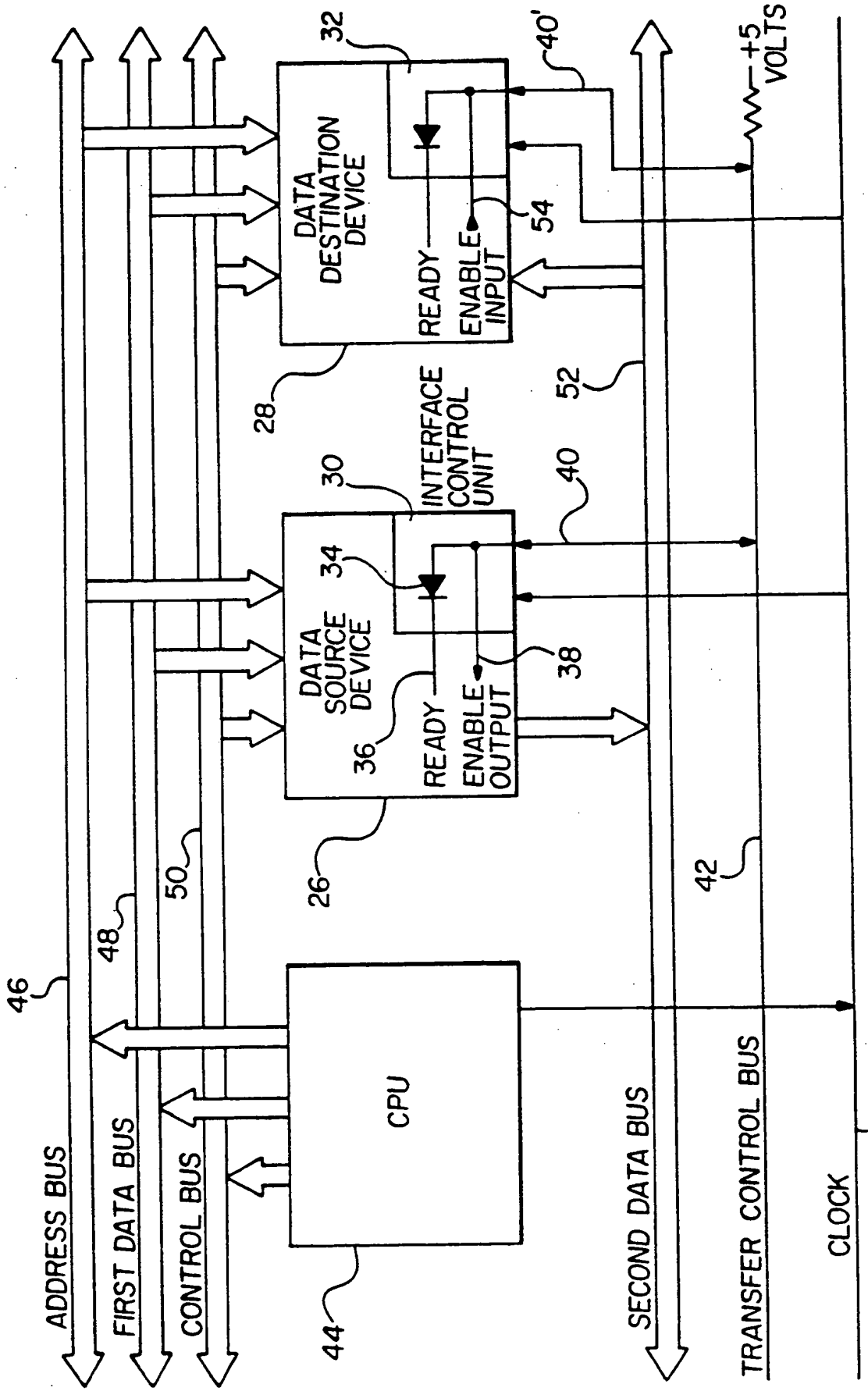
DATA DESTINATION DEVICE
32
40'
+5 VOLTS
READY
ENABLE INPUT
54
28
INTERFACE CONTROL UNIT
30
52
40
DATA SOURCE DEVICE
34
36
READY
ENABLE OUTPUT
38
26
42
50
48
46
CPU
44
ADDRESS BUS
FIRST DATA BUS
CONTROL BUS
SECOND DATA BUS
TRANSFER CONTROL BUS
CLOCK
56
24

FIG. 3

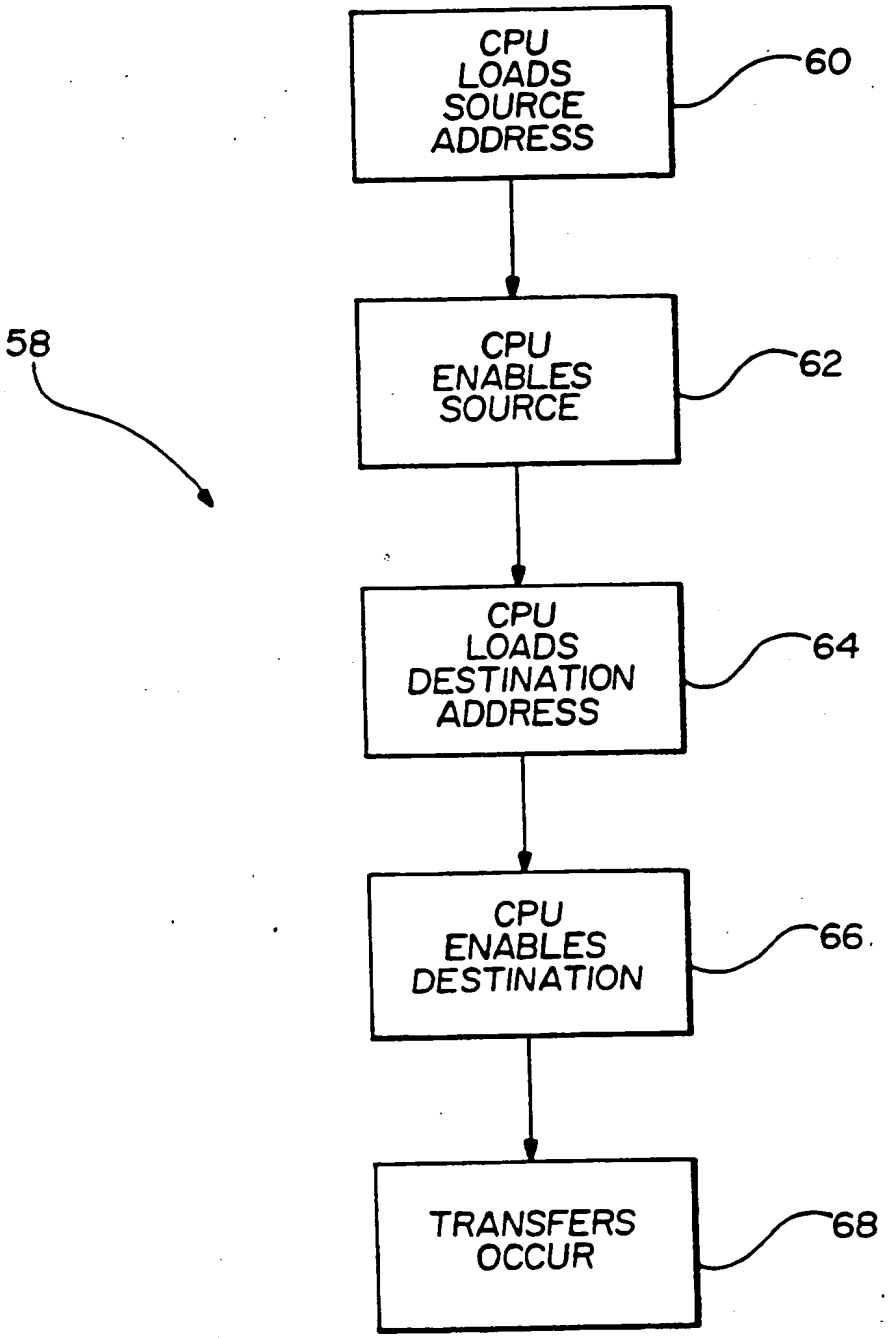
CPU LOADS SOURCE ADDRESS
60
58
CPU ENABLES SOURCE
62
CPU LOADS DESTINATION ADDRESS
64
CPU ENABLES DESTINATION
66
TRANSFERS OCCUR
68

FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 92/03977

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 G06F13/42

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	G06F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X	US,A,4 245 301 (ROKUTANDA ET AL.) 13 January 1981	1-2
Y	see column 1, line 56 - line 60	3
A	see column 2, line 7 - line 22 see column 3, line 20 - line 48 see claim 1; figure 3	4-5

X	EP,A,0 303 751 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 22 February 1989	1-2
A	see column 1, line 52 - column 3, line 8 see column 3, line 47 - column 5, line 32 see figures 1-2	3-5

X	US,A,4 245 307 (KAPEGHIAN ET AL.) 13 January 1981	1-2
A	see column 2, line 23 - line 45 see column 3, line 30 - column 4, line 32 see figure 1	4-5

	-/--	

° Special categories of cited documents :[10]

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
22 SEPTEMBER 1992	01. 10. 92
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
Y	EP,A,0 352 081 (DIGITAL EQUIPMENT CORPORATION) 24 January 1990	3
A	see column 1, line 16 - line 33 see column 2, line 37 - line 63 see column 3, line 24 - line 59 see figure 1	1-2,4-5

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 9203977 SA 60575

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 22/09/92
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-4245301	13-01-81	JP-A- 54027741	02-03-79
EP-A-0303751	22-02-89	JP-A- 1055668	02-03-89
		US-A- 4999769	12-03-91
US-A-4245307	13-01-81	None	
EP-A-0352081	24-01-90	US-A- 5040109	13-08-91
		JP-A- 2176846	10-07-90